AMENDMENTS TO THE CLAIMS

1. (Withdrawn) An integrated circuit (IC), including circuitry arranged in an array having a plurality of rows and a plurality of columns, wherein each row of the plurality of rows begins at a first side of the IC and ends at a second side of the IC, and each column of the plurality of columns begins at a third side of the IC and ends at a fourth side of the IC, the IC comprising:

a column of the plurality of columns comprising a plurality of circuit elements of a circuit type substantially occupying the column; and

a row of the plurality of rows positioned at the third side of the IC, wherein a number of circuit elements of an input and output circuit type in the row is less than a number of remaining circuit elements of other circuit types in the row ; and

a configuration column comprising configuration logic for configuring the column of the plurality of columns.

2. (Withdrawn) The integrated circuit of claim 1 wherein the circuit type is selected from a group consisting of a Configurable Logic Block (CLB) type, a Multi-Giga Bit Transceiver (MGT) type, a Block Random Access Memory (BRAM) type, a Digital Signal Processor (DSP) circuit type, a multiplier circuit type, an arithmetic circuit type, an Input/Output Interconnect (IOI) circuit type, an Input/Output Block (IOB) type, and an application specific circuit type.

3. (Withdrawn) The integrated circuit of claim 1 wherein the input and output circuit type is an Input/Output Block (IOB) type, the IOB configured to input or output data signals into or out of the IC.

4. (Withdrawn) The integrated circuit of claim 1 wherein the input and output circuit type includes an Input/Output Block type and a Multi-Giga Bit Transceiver type.

5. (Withdrawn) The integrated circuit of claim 1 further comprising a center column comprising configuration logic.

6. (Withdrawn) The integrated circuit of claim 3 wherein the center column is positioned on or near the center axis of the IC.

7. (Withdrawn) The integrated circuit of claim 4 further comprising a clock column adjacent to the center column.

8. (Withdrawn) The integrated circuit of claim 1 wherein the column of the plurality of columns further comprises a spacer tile and a clock tile.

9. (Withdrawn) The integrated circuit of claim 1 further comprising an embedded processor.

10. (Currently Amended) An integrated circuit (IC) comprising circuitry having programmable functions and programmable interconnects, the IC further comprising:

a plurality of homogeneous columns and

wherein each of the homogeneous columns starts at one side of the IC and ends at an opposite side of the IC, and

wherein a first column of the plurality of homogeneous columns comprises a first set of substantially identical circuit elements of a first circuit type substantially filling the first column; [[and]]

a heterogeneous column having configuration logic and a clock management circuit element[[.]];

wherein a second column of the plurality of homogeneous columns comprises a second set of substantially identical circuit elements of a second circuit type substantially filling the second column,

a third column of the plurality of homogeneous columns comprises a third set of substantially identical circuit elements of a third circuit type substantially filling the third column,

the first, second, and third circuit types are different from one another,

at least one of the first, second, and third circuit types is an Input/Output Block (IOB) type, and each circuit element of an IOB type provides a circuit interface to

circuitry external to the integrated circuit, and

a column of IOB type circuit elements is between two columns that are not columns having IOB type circuit elements.

Claim 11. (Cancelled)

12. (Previously Presented) The integrated circuit of claim 10 wherein the heterogeneous center column further comprises an input/output block.

13. (Currently Amended) The integrated circuit of claim 10 wherein the first circuit type is selected from a group consisting of a Configurable Logic Block (CLB) type, a Multi-Giga Bit Transceiver (MGT) type, a Block Random Access Memory (BRAM) type, a fixed logic type, an Input/Output Interconnect (IOI) circuit type~~, and an Input/Output Block (IOB) type~~.

14. (Original) The integrated circuit of claim 13 wherein the fixed logic type comprises a Digital Signal Processor (DSP) circuit type, a multiplier circuit type, an arithmetic circuit type, and an application specific circuit type.

15. (Original) The integrated circuit (IC) of claim 10 wherein the integrated circuit further comprises a field programmable gate array (FPGA).

16. (Original) The integrated circuit (IC) of claim 10 wherein the integrated circuit further comprises a programmable logic device (PLD).

Claims 17-23. (Cancelled)

24. (Currently Amended) An integrated circuit (IC) comprising:

a heterogeneous center column having configuration logic and a clock management circuit element;

a plurality of columns and

wherein each of the columns starts at one side of the IC and ends at an opposite side of the IC,

wherein a first column of the plurality of columns comprises a first set of substantially identical circuit elements of a first circuit type substantially filling the first column,

wherein a second column of the plurality of columns comprises a second set of substantially identical circuit elements of a second circuit type substantially filling the second column[[.]]; and

wherein the first and second circuit types are different from one another,

at least one of the first and second circuit types is an Input/Output Block (IOB) type, and each circuit element of an IOB type provides a circuit interface to circuitry external to the integrated circuit, and

a column of IOB type circuit elements is between two columns that are not columns having IOB type circuit elements.

25. (Original) The integrated circuit of claim 24 further comprising circuitry having programmable functions and programmable interconnects.

26. (Currently Amended) The integrated circuit of claim 25 wherein at least one of the first[[,]] and second[[,]] circuit types is [[have]] a circuit type selected from a group consisting of a Configurable Logic Block (CLB) type, a Multi-Giga Bit Transceiver (MGT) type, a Block Random Access Memory (BRAM) type, a Digital Signal Processor (DSP) circuit type, a multiplier circuit type, an arithmetic circuit type, an Input/Output Interconnect (IOI) circuit type, ~~an Input/Output Block (IOB) type,~~ and an application specific circuit type.

Claim 27. (Cancelled)

28. (Original) The integrated circuit of claim 24 wherein the substantially identical circuit elements are substantially identical tiles.

29. (Original) The integrated circuit of claim 28 wherein each tile comprises a functional element coupled to a switch matrix.

Claims 30-36. (Cancelled)

37. (New) The integrated circuit of claim 10, wherein the clock management circuit element in the heterogeneous column performs clock de-skew, clock phase shifting, and clock frequency synthesis.

38. (New) The integrated circuit of claim 37, wherein the configuration logic in the heterogeneous column performs addressing and loading of configuration memory cells for the programmable functions and programmable interconnects of the IC.

39. (New) The integrated circuit of claim 24, wherein the clock management circuit element in the heterogeneous center column performs clock de-skew, clock phase shifting, and clock frequency synthesis.

40. (New) The integrated circuit of claim 39, wherein the configuration logic in the heterogeneous center column performs addressing and loading of configuration memory cells in the IC.